McGINN & GIBB, PLLC
A PROFESSIONAL LIMITED LIABILITY COMPANY
PATENTS, TRADEMARKS, COPYRIGHTS, AND INTELLECTUAL PROPERTY LAW
8321 OLD COURTHOUSE ROAD, SUITE 200
VIENNA, VIRGINIA 22182-3817
TELEPHONE (703) 761-4100
FACSIMILE (703) 761-2375

APPLICATION
FOR
UNITED STATES
LETTERS PATENT

APPLICANT: Kenji Uchida

FOR: CIRCUIT AND METHOD FOR GENERATING FIXED POINT DATA WITH REDUCED CIRCUIT SCALE

DOCKET NO.: NEC-5084-US

CIRCUIT AND METHOD FOR GENERATING FIXED POINT DATA WITH REDUCED CIRCUIT SCALE

Field of the Invention

The present invention relates generally to a circuit and method for generating fixed point data from floating point data with reduced circuit scale. More particularly, the present invention relates to a circuit and method for generating fixed point data to be inputted to a Viterbi decoder in Wide-Band Code Division Multiple Access (hereafter, referred to as W-CDMA) system, from floating point data.

Background of the Invention

Fig. 9 is a schematic block diagram showing an example of a conventional circuit which produces fixed point data from floating point data and performs Viterbi decoding. The circuit of Fig. 9 includes an optimizing circuit 101 and a Viterbi decoder or Viterbi decoding circuit 102. Fig. 10 is a flow chart used for explaining a method of producing fixed point data from floating point data and performing Viterbi decoding, by using the circuit shown in Fig. 9.

In the conventional example shown in Fig. 9 and Fig. 10, floating point data is inputted to the optimizing circuit 101 (step S101), and the inputted floating point data is first converted into fixed point data by using the following formula (step S102), in the optimizing circuit 101.

$$(\text{input data}/\text{MAX data}) \times 2^{(\text{Viterbi input bit width} - 1)} \quad \ldots (1)$$

where "MAX data" is the maximum data among the inputted floating point data.

The fixed point data converted by the above formula is inputted into the Viterbi decoding circuit 102 (step S103), and, in the Viterbi decoding circuit 102, Viterbi decoding is performed by using the inputted fixed point data (step S104).

Thereafter, the result of Viterbi decoding obtained in step S104 is outputted from the Viterbi decoding circuit 102 (step S105).

However, in the above-mentioned conventional circuit, it is necessary to provide a division circuit for performing division process in the optimizing circuit which produces the fixed point data from the inputted floating point data. Therefore, there is a problem that a circuit scale of the fixed point data generating circuit becomes large.

Also, there is another problem that, since the bit width of Viterbi input data is fixed, it is only possible to improve Viterbi decoding rate within the decoding precision corresponding to the fixed bit width.

Summary of the Invention

(Object of the Invention)

Considering the above-mentioned problems of the conventional technology, the present invention has been thought out.

It is an object of the present invention to provide a circuit and method of generating fixed point data from floating point data in which a circuit scale can be reduced.

It is another object of the present invention to provide a circuit and method of generating fixed point data from floating point data in which the bit decoding rate can be improved.

It is still another object of the present invention to provide a circuit and method of generating fixed point data from floating point data in which the bit decoding rate can be improved while reducing a circuit scale.

It is still another object of the present invention to obviate the disadvantages of the conventional circuit and method of generating fixed point data from floating point data.

(Constitution)

According to an aspect of the present invention, there is provided a fixed point data generating circuit which receives a plurality of floating point data and which converts the plurality of floating point data into respective fixed point data, the fixed point data generating circuit comprising: a reference data determining means which determines a reference floating point data from the plurality of floating point data; an exponent part subtractor means which obtains a difference between each of values of exponent parts of the plurality of inputted floating point data and a value of an exponent part of the reference floating point data; a shifting means which shifts a mantissa part of each of the floating point data by the difference obtained by the exponent part subtracting means; and a bit extracting means which extracts a predetermined number of bits of the mantissa part shifted by the shifting means as fixed point data.

In this case, it is preferable that the reference data determining means is a maximum value detecting means which detects the maximum value among the plurality of floating

point data and the reference floating point data is the maximum data among the plurality of floating point data.

It is also preferable that the reference data determining means is a minimum value detecting means which detects the minimum value among the plurality of floating point data and the reference floating point data is the minimum data among the plurality of floating point data.

It is further preferable that the reference data determining means is an average value calculating means which calculates an average value of the floating point data and the reference floating point data is the average data of the plurality of floating point data.

It is advantageous that the bit extracting means extracts bits as the fixed point data from a predetermined location.

It is also advantageous that, when an overflow occurs in the bits extracted by the bit extracting means as the fixed point data, the bits extracted are caused to represent the maximum value thereby.

It is further advantageous that, when an overflow occurs by shifting a mantissa part of each of the floating point data by the shifting means, shifted bits are caused to represent the maximum value thereby.

It is preferable that the fixed point data extracted by the bit extracting means is inputted to a Viterbi decoder.

It is also preferable that location of bits extracted by the bit extracting means as the fixed point data is previously determined to be location having high decoding rate.

According to another aspect of the present invention, there is provided a method for generating fixed point data in which a plurality of floating point data are converted into

respective fixed point data, the method comprising: determining a reference floating point data from the plurality of floating point data; obtaining a difference between each of values of exponent parts of the plurality of inputted floating point data and a value of an exponent part of the reference floating point data; shifting a mantissa part of each of the floating point data by the difference between each of values of exponent parts of the plurality of inputted floating point data and a value of an exponent part of the reference floating point data; and extracting a predetermined number of bits from the mantissa part shifted by the difference as fixed point data.

In this case, it is preferable that the reference floating point data is the maximum data among the plurality of floating point data.

It is also preferable that the reference floating point data is the minimum data among the plurality of floating point data.

It is further preferable that the reference floating point data is the average data of the plurality of floating point data.

It is advantageous that, in the extracting a predetermined number of bits from the mantissa part shifted by the difference as the fixed point data, the bits are extracted from a predetermined location.

It is also advantageous that, in the operation of extracting a predetermined number of bits from the mantissa part shifted by the difference as the fixed point data, when an overflow occurs in the extracted bits, the extracted bits are caused to represent the maximum value thereby.

It is further advantageous that, in the operation of shifting a mantissa part of each of the floating point data by the difference, when an overflow occurs by shifting a mantissa part

of each of the floating point data, shifted bits are caused to represent the maximum value thereby.

It is preferable that the fixed point data extracted in the operation of extracting a predetermined number of bits from the mantissa part shifted by the difference is inputted to a Viterbi decoder.

It is also preferable that location of bits extracted in the operation of extracting a predetermined number of bits from the mantissa part shifted by the difference is previously determined to be location having high decoding rate.

(Operation)

In the floating point data generating circuit according to the present invention which is constituted as mentioned above, when a plurality of floating point data are inputted thereto, a reference data such as the maximum or minimum floating point data is first detected from among the plurality of floating point data. A difference is obtained between the value of an exponent part of each of the inputted plurality of floating point data and the value of an exponent part of the maximum or minimum floating point data. Thereafter, a mantissa portion of each of the inputted floating point data is shifted by the amount of the difference, and a predetermined number of bits of the shifted mantissa are extracted as the fixed point data.

In this way, according to the present invention, fixed point data are produced from floating point data, only by comparison and subtraction process of the inputted floating point data. Therefore, a circuit scale does not become large.

Also, it is possible to use an average value of the inputted plurality of floating point data as a reference data. In this

case, a difference is obtained between the value of an exponent part of the average value and the value of an exponent part of each of the inputted plurality of floating point data, the mantissa part of each of the floating point data is shifted by the amount of the difference, and a predetermined number of bits among the shifted mantissa can be extracted as the fixed point data.

Further, in case location of bits extracted as the fixed point data is previously determined to be location having high decoding rate, it is possible to improve the decoding rate.

Brief Description of the Drawings

These and other features, and advantages, of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which like reference numerals designate identical or corresponding parts throughout the figures, and in which:

Fig. 1 is a schematic block diagram showing a fixed point data generating circuit according a first embodiment of the present invention;

Fig. 2 is a flow chart used for explaining a method of generating fixed point data from floating point data, in the fixed point data generating circuit shown in Fig. 1;

Fig. 3 is a graph showing circuit scales of a fixed point data generating circuit which uses a subtractor and of a fixed point data generating circuit which uses a dividing circuit;

Fig. 4 is a graph showing bit error rate (BER) characteristic of each of the fixed point data generating circuit

shown in Fig. 1 and a conventional fixed point data generating circuit;

Fig. 5 is a schematic block diagram showing a fixed point data generating circuit according a second embodiment of the present invention;

Fig. 6 is a flow chart used for explaining a method of generating fixed point data from floating point data in the fixed point data generating circuit shown in Fig. 5;

Fig. 7 is a schematic block diagram showing a fixed point data generating circuit according to a third embodiment of the present invention;

Fig. 8 is a flow chart used for explaining a method of generating fixed point data in the fixed point data generating circuit shown in Fig. 7;

Fig. 9 is a schematic block diagram showing an example of a conventional circuit which produces fixed point data from floating point data and performs Viterbi decoding; and

Fig. 10 is a flow chart for explaining a method of producing fixed point data from floating point data and performing Viterbi decoding by using the circuit shown in Fig. 9.

Description of a Preferred Embodiment

Hereafter, embodiments of the present invention will be described with reference to the drawings.

(First embodiment)

Fig. 1 is a schematic block circuit diagram showing a fixed point data generating circuit according to a first

embodiment of the present invention.

As shown in Fig. 1, the fixed point data generating circuit according to the first embodiment of the present invention comprises: a MAX (i.e., maximum) value detecting circuit 10 which detects the maximum floating point data as a reference data among inputted floating point data which are inputted to the MAX value detecting circuit 10; an exponent part subtractor 20 which subtracts the value of an exponent part of each of the inputted floating point data from the value of an exponent part of the floating point data which is detected as the maximum value at the MAX value detecting circuit 10; a shift register 30 which shifts the value of a mantissa part of each of the inputted floating point data based on the result of subtraction at the exponent part subtractor 20; and a bit extracting portion 40 which extracts, from the mantissa part shifted by the shift register 30, a predetermined number of bits as the fixed point data to be inputted to a Viterbi decoding circuit (not shown in the drawing).

With reference to a flow chart, an explanation will be made on a method of generating the fixed point data in the fixed point data generating circuit which is constituted as mentioned above.

Fig. 2 is the flow chart used for explaining the method of generating the fixed point data from inputted floating point data, in the fixed point data generating circuit shown in Fig. 1.

Floating point data are inputted to the circuit of Fig. 1 (step S1), and, first, in the MAX value detecting circuit 10, the maximum floating point data D_{max} is detected among the inputted floating point data D1, D2, D3, ... , Dn as follows (step S2).

$$D_{max}=\max\{D1, D2, D3, \ldots, Dn\} \quad \text{(n: amount of data)} \quad \ldots (1)$$
$$(D_{max}=D_{maxM(mantissa)} \times 2^{DmaxE(exponent)})$$

Next, in order to adjust the exponent part of each of the inputted floating point data to the maximum value, the value of the exponent part of each of the inputted floating point data is subtracted from the value of the exponent part of the floating point data detected as the maximum value at the MAX value detecting circuit 10, at the exponent part subtractor 20, and outputted as a quantity of shift (step S3).

$$\text{Quantity of shift} = D_{maxE} - D_{inE} \quad \ldots. (3)$$
(D_{maxE} : maximum exponent value, D_{inE} : exponent value of inputted floating point data)

In the shift register 30, the value of the mantissa part of each of the inputted floating point data is shifted, based on the quantity of shift calculated by the equation (3) (step S4).

$$\text{Fixed point data}=D_{inM}/2^{(\text{quantity of shift})} \quad \ldots (4)$$
(D_{inM} : mantissa value of the inputted floating point data)

Then, in the bit extracting portion 40, a predetermined number of bits are extracted from the mantissa part which is shifted in the shift register 30 as the fixed point data to be inputted to the Viterbi decoding circuit (step S5). In this case, by fixing the location of bits to be extracted to bit location having high decoding rate, it is possible to improve the precision of decoding.

In the bit extracting portion 40, when an overflow occurs in the extracted bits, saturation processing is performed by representing the maximum value by using the extracted bits (step S6), and thereby optimization of data is attained.

Thereafter, the fixed point data extracted in the bit extracting portion 40 is inputted to the Viterbi decoding circuit (step S7), and, in the Viterbi decoding circuit, Viterbi decoding is performed by using the inputted fixed point data (step S8).

Hereafter, an explanation will be made on the above-mentioned series of processings, by way of example when four (4) bit data is supplied to the Viterbi decoding circuit.

The inputted data is assumed to be as follows. That is, a mantissa part (including a sign bit) is 8 bits in length, an exponent part is 4 bits in length, and the output is 4 bits. Also, it is assumed that the following three floating point data are inputted.

Mantissa part | Exponent part
#1: 0110 0100 | 0100 = 100 x 2^4 = 1600
#2: 0110 0000 | 0110 = 96 x 2^6 = 6144
#3: 0110 1000 | 0101 = 104 x 2^5 = 3328

First, in the MAX value detecting circuit 10, the maximum floating point data is detected among the inputted floating point data. Here, the maximum floating point data among the three floating point data mentioned above becomes data #2, and, therefore, floating point data #2 is detected as the maximum data.

Next, in the exponent part subtractor 20, in order to adjust the exponent parts of all the inputted floating point data

to the same value, the values of the exponent parts of the inputted floating point data are subtracted from the value of the exponent part of the maximum floating point data #2. In the above-mentioned three floating point data, such subtraction becomes as follows.

#2 - #1 = 0110 - 0100 = 0010
#2 - #3 = 0110 - 0101 = 0001

In the shift register 30, based on the above-mentioned subtraction result, the mantissa parts of the floating point data #1 and #3 are shifted, and, thereby, each of the floating point data #1 and #3 is represented by using the same exponent as that of the floating point data #2.

That is, according to the result of the following calculation:

#2 - #1 = 0110 - 0100 = 0010,

the value of the mantissa part of the floating point data #1 is shifted by 2 bits. Also, according to the result of the following calculation:

#2 - #3 = 0110 - 0101 = 0001,

the value of the mantissa part of the floating point data #3 is shifted by 1 bit.

Thereby, the following result is obtained.

Mantissa part | Exponent part

#1: 0001 1001 | 0110 = 25 x 2^6 = 1600
(mantissa part: shifted by 2 bits)
#2: 0110 0000 | 0110 = 96 x 2^6 = 6144
#3: 0011 0100 | 0110 = 52 x 2^6 = 3328
(mantissa part: shifted by 1 bit)

Thereafter, in the bit extracting portion 40, for each of the floating point data #1 to #3, a predetermined number of output bits are extracted from the MSB bit side, and extracted bits are used as the input data to the Viterbi decoding circuit.

Mantissa part | Viterbi input data (4 bits)
#1: <u>0001</u> 1001 | to 0001
#2: <u>0110</u> 0000 | to 0110
#3: <u>0011</u> 0100 | to 0011

The above-mentioned series of processings can be realized by using a subtractor having a bit length of bits of an exponent part, a comparator and a shift register.

Also, by making lower bits other than the bits extracted by the bit extracting portion 40 effective, it is possible to improve precision of Viterbi decoding.

An explanation will be made below on bit extraction processing in the bit extracting portion 40 which improves the precision of Viterbi decoding.

In the bit extraction processing, it is possible to change the location of data bits to be extracted in the bit extracting portion 40 in order to make the lower bit or bits effective, and thereby to improve the precision of Viterbi decoding.

An explanation of the bit extraction processing will be

described by way of concrete example.

In the above-mentioned data:

Mantissa part	Exponent part
#1: 0001 1001	0110 = 25 x 2^6 = 1600 (mantissa part: shifted by 2 bits)
#2: 0110 0000	0110 = 96 x 2^6 = 6144
#3: 0011 0100	0110 = 52 x 2^6 = 3328 (mantissa part: shifted by 1 bit),

the bits to be extracted by the bit extracting portion 40 are determined to be bits whose leading bit is the second bit from the MSB (except the sign bit), and the following result is obtained.

Mantissa part	Viterbi input data (4 bits)
#1: 0001 1001	to 0011
#2: 0110 0000	to 0100
#3: 0011 0100	to 0110

Here, since there is an overflow in #2, that is, since the MSB bit (except the sign bit) is "1", the maximum value is represented within the bits of the data #2 to perform a saturation processing.

Mantissa part	Viterbi input data (4 bits)
#1: 0001 1001	to 0011
#2: 0110 0000	to 0111 (saturation processing)
#3: 0011 0100	to 0110

When determining the bits to be extracted in the bit extracting portion 40, it is preferable to set the bit location to be extracted by using a parameter showing the bit location, and to determine the parameter corresponding to a high Viterbi decoding rate as a fixed value.

Fig. 3 is a graph showing a circuit scale of each of a fixed point data generating circuit which uses a subtractor and a fixed point data generating circuit which uses a dividing circuit.

As shown in Fig. 3, when compared with the circuit area, i.e., number of circuit cells, of the fixed point data generating circuit which uses a dividing circuit, the circuit area, i.e., number of circuit cells, of the fixed point data generating circuit shown in Fig. 1 which uses a subtractor can be reduced.

Fig. 4 is a graph showing bit error rate (BER) characteristic of each of the fixed point data generating circuit shown in Fig. 1 and the conventional fixed point data generating circuit. Fig. 4 shows decoding rates of respective values of Eb/No (energy versus noise power density per one bit).

In Fig. 4, it is assumed that equal floating point data is inputted to the conventional fixed point data generating circuit and to the fixed point data generating circuit shown in Fig. 1, and that number of input bits to the Viterbi decoding circuit is 8 bits. In this condition, when BER values corresponding to a value of Eb/No are roughly compared, in the proximity of Eb/No=6dB, BER=1.00E-02 in the conventional fixed point data generating circuit (it is impossible to decode one data per 100 number of data). On the other hand, in the fixed point data generating circuit of Fig. 1, BER=1.00E-03 (it is impossible to decode one data per 1000 number of data), and it can be seen that the decoding rate is improved.

(Second embodiment)

Fig. 5 is a schematic block diagram showing a second embodiment of a fixed point data generating circuit according to the present invention.

As shown in Fig. 5, the fixed point data generating circuit according to the second embodiment of the present invention comprises: a MIN (i.e., minimum) value detecting circuit 11 which detects the minimum floating point data among inputted floating point data which are inputted to the MIN value detecting circuit 11; an exponent part subtractor 21 which subtracts the value of an exponent part of the floating point data which is detected as the minimum value at the MIN value detecting circuit 11 from the value of an exponent part of each of the inputted floating point data; a shift register 30 which shifts the value of a mantissa part of each of the inputted floating point data based on the result of subtraction at the exponent part subtractor 21; and a bit extracting portion 40 which extracts, from the mantissa part shifted by the shift register 30, a predetermined number of bits as the fixed point data to be inputted to a Viterbi decoding circuit (not shown in the drawing).

With reference to a flow chart, an explanation will be made on a method of generating the fixed point data in the fixed point data generating circuit which is constituted as mentioned above.

Fig. 6 is the flow chart used for explaining the method of generating the fixed point data in the fixed point data generating circuit shown in Fig. 5.

A plurality of floating point data are inputted to the

circuit of Fig. 5 (step S11), and, first, in the MIN value detecting circuit 11, the minimum floating point data D_{min} is detected among the inputted floating point data D1, D2, D3, ... , Dn (step S12).

$$D_{min}=\min\{D1, D2, D3, \dots, Dn\} \quad \text{(n: amount of data)} \quad \dots (5)$$
$$(D_{min}=D_{minM(mantissa)} \times 2^{DminE(exponent)})$$

Next, in order to adjust the exponent part of each of the inputted floating point data to the minimum value, the value of the exponent part of the floating point data detected as the minimum value at the MIN value detecting circuit 11 is subtracted from the value of the exponent part of each of the inputted floating point data, at the exponent part subtractor 21, and outputted as a quantity of shift (step S13).

$$\text{Quantity of shift} = D_{inE} - D_{minE} \quad \dots. (6)$$
(D_{minE} : minimum exponent value, D_{inE} : exponent value of inputted floating point data)

In the shift register 30, the value of the mantissa part of each of the inputted floating point data is shifted, based on the quantity of shift calculated by the equation (6) (step S14).

$$\text{Fixed point data}=D_{inM}/2^{(\text{quantity of shift})} \quad \dots (7)$$
(D_{inM} : mantissa value of the inputted floating point data)

Here, when an overflow occurs in the shifted bits, the maximum value is represented within the bits to perform a saturation processing (step S15).

Then, in the bit extracting portion 40, a predetermined number of bits are extracted from the mantissa part which is shifted in the shift register 30 as the fixed point data to be inputted to the Viterbi decoding circuit (step S16). In this case, by fixing the location of bits to be extracted to bit location having a high decoding rate, it is possible to improve the precision of decoding.

In the bit extracting portion 40, when an overflow occurs in the extracted bits, saturation processing is performed by representing the maximum value by using the extracted bits (step S17), and thereby optimization of data is attained.

Thereafter, the fixed point data extracted in the bit extracting portion 40 is inputted to the Viterbi decoding circuit (step S18), and, in the Viterbi decoding circuit, Viterbi decoding is performed by using the inputted fixed point data (step S19).

(Third embodiment)

Fig. 7 is a schematic block diagram showing a third embodiment of a fixed point data generating circuit according to the present invention.

As shown in Fig. 7, the fixed point data generating circuit according to the third embodiment of the present invention comprises: an average value calculating circuit 12 which calculates an average value of inputted floating point data which are inputted to the average value calculating circuit 12; an exponent part subtractor 22 which obtains a difference between each value of an exponent part of the inputted floating point data and the value of the average value calculated by the average value detecting circuit 12; a shift register 30 which shifts the value of a mantissa part of the inputted floating point

data based on the difference obtained in the exponent part subtractor 22; and a bit extracting portion 40 which extracts, from the mantissa part shifted by the shift register 30, a predetermined number of bits as the fixed point data to be inputted to a Viterbi decoding circuit (not shown in the drawing).

With reference to a flow chart, an explanation will be made on a method of generating the fixed point data in the fixed point data generating circuit which is constituted as mentioned above.

Fig. 8 is the flow chart used for explaining the method of generating the fixed point data in the fixed point data generating circuit shown in Fig. 7.

A plurality of floating point data are inputted to the circuit of Fig. 7 (step S21), and, first, in the average value calculating circuit 12, the average value D_{ave} of the inputted floating point data D1, D2, D3, ... , Dn is calculated (step S22).

$$D_{ave}=\text{average}\{D1, D2, D3, \ldots, Dn\} \quad \text{(n: amount of data)} \quad \ldots (8)$$
$$(D_{ave}=D_{aveM(mantissa)} \times 2^{DaveE(exponent)})$$

Next, in order to adjust the exponent parts of the inputted floating point data to the exponent value of the average value, a difference is obtained between the value of the exponent part of each of the inputted floating point data and the exponent part of the average value calculated in the average value detecting circuit 12, at the exponent part subtractor 22, and outputted as a quantity of shift (step S23).

$$\text{Quantity of shift} = D_{aveE} - D_{inE} \ \ldots. (9)$$

(D_{aveE} : average exponent value, D_{inE} : exponent value of inputted floating point data)

In the shift register 30, the value of the mantissa part of each of the inputted floating point data is shifted, based on the quantity of shift calculated by the equation (9) (step S24). Here, when the quantity of shift is calculated by using the average value of the floating point data like the present embodiment, there is a possibility that the value of the mantissa part shifts in either of the MSB bit side and the LSB bit side. Therefore, concerning an operation of the shift register 30 when the fixed point data is calculated, the following two formulas become true.

(exponent value of average data >exponent value of inputted floating point data)

$$\text{Fixed point data} = D_{inM}/2^{(\text{quantity of shift})} \quad \dots (10)$$

(D_{inM} : mantissa value of the inputted floating point data)

(exponent value of average data <exponent value of inputted floating point data)

$$\text{Fixed point data} = D_{inM} \times 2^{(\text{quantity of shift})} \quad \dots (11)$$

(D_{inM} : mantissa value of the inputted floating point data)

Also, when an overflow occurs in the shifted bits, the maximum value is represented within the bits to perform a saturation processing (step S25).

Then, in the bit extracting portion 40, a predetermined number of bits are extracted from the mantissa part which is shifted in the shift register 30 as the fixed point data to be

inputted to the Viterbi decoding circuit (step S26). In this case, by fixing the location of bits to be extracted to bit location having a high decoding rate, it is possible to improve the precision of decoding.

In the bit extracting portion 40, when an overflow occurs in the extracted bits, saturation processing is performed by representing the maximum value by using the extracted bits (step S27), and thereby optimization of data is attained.

Thereafter, the fixed point data extracted in the bit extracting portion 40 is inputted to the Viterbi decoding circuit (step S28), and, in the Viterbi decoding circuit, Viterbi decoding is performed by using the inputted fixed point data (step S29).

(Effect of the Invention)

As mentioned above, in the present invention, a reference floating point data which has the maximum or minimum value is detected among the inputted plurality of floating point data, and differences are obtained between the values of the exponent parts of a plurality of inputted floating point data and the exponent value of the maximum or minimum floating point data. Thereafter, the mantissa parts of the inputted floating point data are shifted by the differences, and a predetermined number of bits of the shifted mantissa parts are extracted as the fixed point data. Therefore, it is possible to produce the fixed point data only by the comparison and subtraction of the inputted floating point data, so that it becomes possible to perform optimization with respect to the inputted floating point data and to reduce a circuit scale.

Also, in case an average value of inputted plurality of floating point data is calculated and differences are obtained

between the value of an exponent part of the average value and the values of exponent parts of the inputted plurality of floating point data, effects similar to those mentioned above can be obtained.

Further, in case location of bits extracted as the fixed point data is previously determined to be location having a high decoding rate, it is possible to improve the decoding rate.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. For example, in the above-mentioned embodiments, the maximum, minimum or average data are obtained from the inputted floating point data and used as a reference data. However, it is also possible to use any other data obtained from the inputted floating point data as a reference data. For example, it is possible to use the median obtained from the inputted floating point data as the reference data, in place of the maximum, minimum or average data.

Accordingly, the specification and figures are to be regarded in an illustrative sense rather than a restrictive sense, and all such modifications are to be included within the scope of the present invention. Therefore, it is intended that this invention encompasses all of the variations and modifications as fall within the scope of the appended claims.